Amendments to the Claims:

This listing of claims will replace all prior versions and listings of the claims in the application:

1. (original) A data processor having a semiconductor chip, comprising:

a central processing unit;

an interface controller to perform input and output of data to and from an external side of the semiconductor chip; and

a bus controller connected with an external bus,

wherein said interface controller includes an interface control unit, a FIFO unit, and a transfer control unit,

wherein said interface control unit outputs the data of said FIFO unit to an external side of said semiconductor chip and inputs the data inputted from the external side of said semiconductor chip to said FIFO unit, and

wherein said transfer control unit performs the control to transfer the data stored in the FIFO unit by designating a transfer destination address and the control to input the data to the FIFO unit by designating a transfer source address.

2. (original) The data processor according to claim 1, wherein said transfer control unit designates the transfer destination address for storing the data in parallel to the read of data from said FIFO unit.

3. (original) The data processor according to claim 1, wherein said transfer control unit inputs the data to said FIFO unit in parallel to the read of data from the designated transfer source address.

4. (currently amended) The data processor according to ~~any one of claims 1 to 3~~ claim 1, wherein said interface controller is a USB interface controller.

5. (original) A data processor having a semiconductor chip, comprising:

a central processing unit;

an interface controller for inputting and outputting data from and to an external side of the semiconductor chip;

a data transfer control device for interface controller;

a bus controller connected to an external bus; and

a general purpose transf r control devic for controlling the data transfer to the external bus via said bus controller,

wherein said interface controller includes an interface control unit and a FIFO unit,

wherein said interface control unit outputs the data of the FIFO unit to the external side of said semiconductor chip and inputs the data inputted from the external side of said semiconductor chip to said FIFO unit, and

wherein said data transfer control device for interface controller performs the control to transfer the data stored in said FIFO unit by designating a transfer destination address and the control to input the data to said FIFO unit by designating a transfer source address.

6. (original) The data processor according to claim 5, wherein said data transfer control device for interface controller designates the transfer destination address for storing the data in parallel to the read of data from said FIFO unit.

7. (original) The data processor according to claim 5, wherein said data transfer control device for interfac

controller inputs the data to said FIFO unit in parall l to the read of data from the designated transfer source address.

8. (original) A data processor having a semiconductor chip, comprising:

a central processing unit;

an interface controller for inputting and outputting data from and to an external side of the semiconductor chip;

a bus controller connected to an external bus;

a data transfer control device for controlling data transfer to said external bus via said bus controller; and

a RAM,

wherein said interface controller includes an interface control unit and a transfer control unit,

wherein said interface control unit outputs the data stored in a predetermined region of said RAM to the external side of said semiconductor chip and inputs the data inputted from the external side of said semiconductor chip to the predetermined region of said RAM, and

wherein said transfer control unit performs the control to transfer th data stored in the predetermined

region of said RAM by designating th transfer destination address and the control to input the data in the predetermined region of said RAM by designating the transfer source address.

9. (original) The data processor according to claim 8, wherein said transfer control unit individually includes a first address generating unit to generate the address for making access in a FIFO format to the predetermined region of said RAM and a second address generating unit to generate the address for making access via the external bus through said bus controller.

10. (original) The data processor according to claim 9, wherein said transfer control unit reads the data from the address designated by said first address generating unit in the former half of a transfer cycle and writes the data to the address designated by said second address generating unit in the latter half of the transfer cycle.

11. (original) A data processor formed over a semiconductor substrate, comprising:

a CPU:

a USB controll r;

a DMA controller; and

an internal bus coupled to said CPU, said USB controller, and said DMA controller,

wherein said USB controller includes a FIFO buffer and a data transfer control device which can execute transfer control of the data stored in said FIFO buffer.

12. (original) The data processor according to claim 11, wherein said data transfer control device has an address generating function to designate the address of said FIFO buffer and designate the address of an external device coupled to said data processor.

13. (original) A data processor formed over a semiconductor substrate, comprising:

a CPU;

a USB controller;

a DMA controller;

a RAM; and

an internal bus coupled to said CPU, said USB controller, said DMA controller, and said RAM,

wherein said USB controller includes a data transfer control device which can execute the transfer control of the data stored in said RAM.

14. (original) The data processor according to claim 13, wherein said data transfer control device includes an address generating function to designate the address of said RAM and designate the address of the external device coupled to said data processor.

15. (original) A data processor formed over a semiconductor chip, comprising:

a general purpose transfer control unit which can execute the data transfer for the external device coupled to a general purpose external bus via this general purpose external bus to be coupled to said data processor; and

a data transfer control unit of a predetermined interface which can execute the data transfer for an external side of said data processor via a predetermined external bus having predetermined specifications to be coupled to said data processor,

wherein said data transfer control unit of said pred termined interface includes an address designating

unit which can designate the address of transfer buffer and also designate the address of said external device.

16. (original) The data processor according to claim 15, wherein said transfer buffer is provided in the data transfer control unit of said predetermined interface.

17. (original) The data processor according to claim 15, further comprising a RAM,

wherein said transfer buffer is designated as a part of region of said RAM.

18. (original) The data processor according to claim 17, wherein said RAM further includes a region designated as the transfer buffer for said general purpose data transfer control unit.

19. (original) The data processor according to claim 15, wherein said address designating unit reads the data from the designated address in the former half of a transfer cycle and writes the data to the designated address in the latter half of the transfer cycle.

20. (n w) The data processor according to claim 2, wherein said interface controller is a USB interface controller.

21. (new) The data processor according to claim 3, wherein said interface controller is a USB interface controller.